SECTION 1 INTRODUCTION

The video system in this game consists of five (5) printed circuit boards, a number of switches, and a Video Monitor. The printed circuit boards contain most of the electronic circuitry in the game. Switches provide controlling inputs for play of the game and the Video Monitor provides a high-resolution color display of game action.

The basic functions of the five circuit boards are as follows. (Refer to Figure 1-1.) The Power Supply provides the necessary voltages for proper game operation. Regulated DC outputs of +5VDC, -5VDC, +12VDC, and unregulated DC outputs of +12VDC, -12VDC, and +27 VDC are supplied. An additional AC output (6.3 VAC) is used to power lamps for general illumination purposes.

The CPU/Video board contains a microcomputer Central Processing Unit (CPU), which performs the "brain" function of the system. The CPU controls the rest of the system according to the program (list of instructions) assigned to it by a programmer. This board also contains the Video Control circuitry and Video Memory. The information stored in the Video Memory represents the picture the CPU wants displayed on the Video Monitor. The Video Control circuits read the contents of the Video Memory and convert these contents into color signals which are then fed to the Video Monitor.

The ROM board provides ROM storage for the programs and data base which control the operation of the Video System and supply the necessary data for game operations. The ROM board contains: the game program, the diagnostic (self-test) programs, permanent data used by programs, and I/O (Input/Output) ports. An Input port is used by the system to check the status of input switches. An Output port is used to control the on-board Self-Test indicator LEDs, and game play-selected sounds produced by the Sound Board.

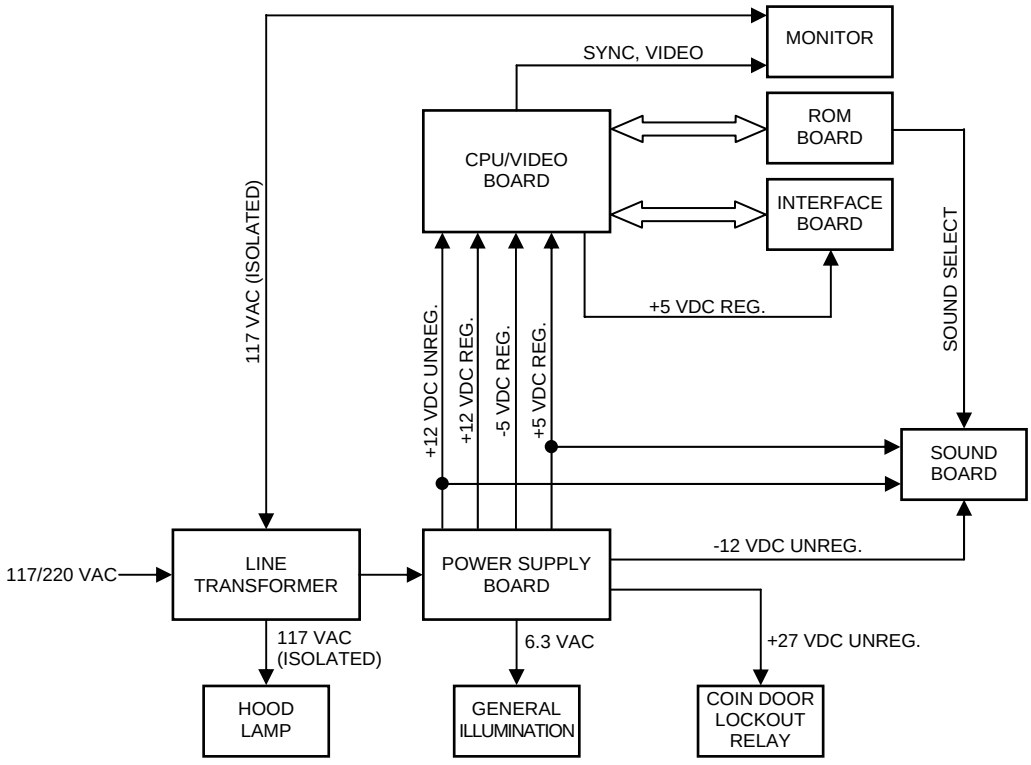

Figure 1-1. Simplified Block Diagram

The Sound Board is able to generate various sound effects upon appropriate command from the CPU. These commands are received via the ROM board. The audio signals generated in response to these commands are amplified on-board, and routed directly to the game speaker system.

The Interface Board provides input ports to interface the Video System to the Player Control Panel. These inputs allow the CPU to check the status of the 1- and 2- player start switches and player panel control switches.

SECTION 2 BLOCK DIAGRAM THEORY

The Williams Video Game System generates a color video display of 360 x 240 pixels (picture elements) on a standard Color Monitor. The Color Monitor provides one complete (non-interlaced) scan of the screen every 16.66 mSec, for a standard frame rate of 60 Hz. The screen may contain up to 16 different colors at once, which are selected under program control from a total of 256 available colors. For each pixel to be displayed, a 4-bit binary code representing one of the 16 currently-available colors is stored in a memory called the Video RAM. These 4-bit pixel codes a r e continuously read out of the Video RAM in the order they are to be displayed, and used as an address to access 1 of 16 8-bit codes stored i n a 16 byte memory called the color RAM. Each of these 16 codes represents 1 of the 256 total available colors (2^8=256). Each 8-bit color code output from the color RAM represents a different combination of brightness levels for the Red, Blue, and Green guns in the monitor, producing 1 of the 256 possible color combinations.

The result is a process of two basic steps for the display of a picture:

1. Select 16 of 256 available colors for the current display by loading the 8-bit value for each color selection in to 1 of the 16 color RAM locations. The address at which each color code is stored determines which 4-bit pixel code will cause it to be displayed.
2. Select which of the 16 currently available colors will be displayed at each pixel location on the screen by storing the appropriate 4-bit codes in the Video RAM.

Figure 2-1 is a block diagram showing the main features of the Williams Video Game System hardware.

The Reset circuit produces 2 reset pulses, $\overline{\text{RESET}}$ (Reset Not) and $\overline{\text{CR}}$ (Clocked Reset Not), in response to either a low supply voltage (power-up or power-down) or the reset pushbutton being depressed. These pulses assure that the MPU (Microprocessor Unit) and critical timing components such as the Video Address Generator are forced into a stable state during power fluctuations or testing, and synchronized when normal operation begins. When there set condition has terminated, a properly functioning MPU will restart the main program, executing system diagnostics and then the game program itself.

The Watchdog circuit is a timer which resets the MPU unless it is cleared before it counts 8 vertical scans. The timer is cleared by writing a specific data pattern at a specific memory address. The command to clear the Watchdog is built into the game program so that during normal game operation the Watchdog is always cleared before it forces the MPU to reset. Should the MPU stop executing the proper instruction sequences and fail to clear the Watchdog, the reset will bring the game up in "Game Over".

The Clock Generator provides basic timing for the video system and consists of a 12MHz oscillator and dividers to 4 MHz and 6 MHz clocks. The $\overline{\text{12 MHz}}$ clock is also applied to the Video RAM Timing Circuit with other derived timing signals to provide timing for access to the Video RAMS. The $\overline{\text{4 MHz}}$ clock signal derives the E and Q clocks required by the MPU, clocks the Video Address Generator, and,(with the $\overline{\text{6 MHz}}$ clock), provides timing for the Video Shift Registers.

The E and Q Generator divides the $\overline{\text{4 MHz}}$ clock to produce E and Q clocks. These 1 MHz clock phases provide the timing for the MPU and are also applied to the Video RAM Timing Circuit.

The Video Address Generator provides the 14 addresses that scan the Video RAM to produce a frame on the monitor 60 times a second. Function $\overline{CR}$, (Clocked Reset Not), is synchronized with the E clock and holds the counter reset when it is low. When it goes high, the 4 MHz clock is counted to produce the addresses. The addresses are applied through the Video Address Multiplexer to scan the Video RAM banks. In addition, an output is applied to the Watchdog circuit and outputs are decoded to provide horizontal and vertical sync for the Color Monitor and blanking in the Video D-to-A Driver.

The three RAM Banks are scanned simultaneously by the Video Address Bus, and individually by the microprocessor.

The Video RAM Control Circuit accepts microprocessor address bits A8 through A15 to address a PROM. The PROM provides pseudo-address bits PA8 through -PA13, and $\overline{E}$ and $\overline{WE}$ (Enable Not and Write Enable Not) functions. This control circuit allows the microprocessor to access the Video RAM Banks individually with sequential addresses. The circuit also provides multiplexing signal MUX 1 to the Video RAM Address Multiplexer.

The Video RAM timing circuit uses the $\overline{12\ MHz}$, E, and Q clocks to produce Video RAM timing. Each Video RAM bank provides 16K address locations, and is accessed with seven address bits at a time. The memory in the RAM is configured in a matrix with 7 of the 14 address bits latched into select a row in the memory matrix and then the remaining 7 address bits latched into select a column.

Function $\overline{RAS}$ (Row Address Select Not) and $\overline{CAS}$ (Column Address Select Not) latch the addresses into the RAM at the proper time. Functions MUX 1 from the Video RAM control circuit and MUX 0 pass high, and low-order video address bits for video access, also low-order microprocessor address bits and pseudo-address bits for microprocessor video access.

Function $\overline{SRL}$ (Shift Register Load Not) latches the data outputs from the three RAM Banks into the Video Shift Register after each video access. Function $\overline{WE}$ is produced at an appropriate time during microprocessor access to enable the $\overline{WE}$ (Write Enable Not) outputs from the Video RAM control circuit.

The Video RAM Address Multiplexer uses the MUX 0 and MUX 1 signals to place appropriate addresses on the Memory Address Bus (MA0 through MA6) for latching by the $\overline{RAS}$ and $\overline{CAS}$ signals.

MUX 0	MUX 1	ADDRESSES	RAM
LOW	LOW	UP AD, Pseud.A8-A13	Row
HIGH	LOW	UP A1-A7	Column
LOW	HIGH	VA0-VA6	Row
HIGH	HIGH	VA7-VA13	Column

Video RAM is accessed by the Video Address Bus every microsecond and the data is latched into the Video Shift Register. When the microprocessor reads from RAM, the $\overline{E}$ (Enable Not) signal from the Video RAM control circuit latches the data from the appropriate RAM Bank in to the MPU Data Bus.

The Video Shift Registers load the data from the RAM Banks into shift registers. Functions $\overline{SRL}$ (Shift Register Load Not) and the $\overline{4\ MHz}$ clock synchronize loading of data into the shift register. The $\overline{6\ MHz}$ clock shifts out the 4-bit sets of data in parallel. The data loaded into the shift registers in sets of four bits define a pixel (picture element). Four bits from RAM Bank 1 are first presented to the Color RAM Address Multiplexer for a pixel. The next $\overline{6\ MHz}$ clock pulse shifts the other 4 bits from RAM Bank 1.

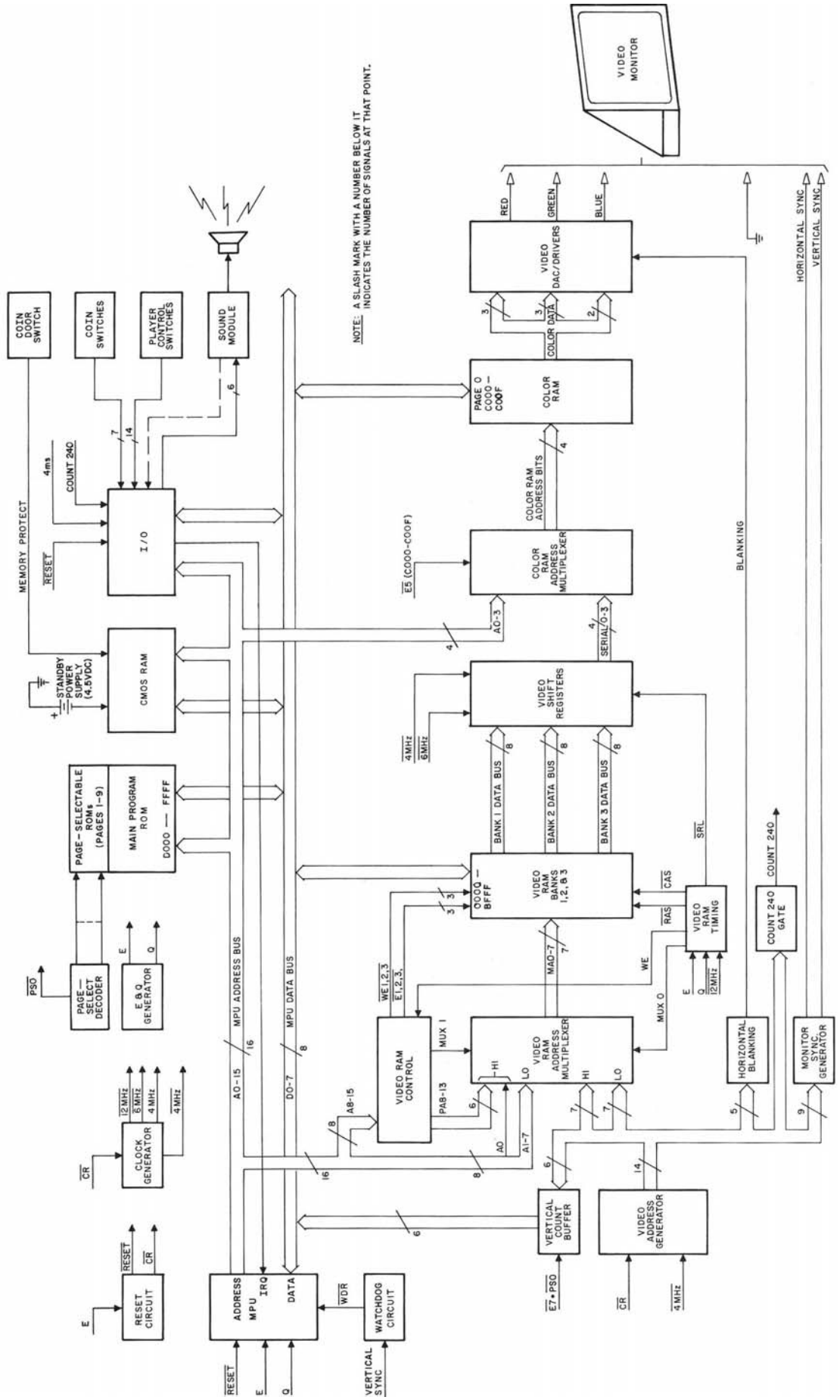

Figure 2-1. Main Features of Williams Video Game System Hardware

The next two clock pulses shift out the bits from RAM Bank 2 and the third and fourth clock pulses, the bits from RAM Bank 3.

Function $\overline{SRL}$ occurs at a 1 MHz rate, loading sets of four bits into the shift register. The $\overline{6\ MHz}$ clock shifts the sets of bits out prior to the next load.

The Color RAM Address Multiplexer passes 4-bit sets from the Video Shift Registers to the color RAM. The color RAM is a 16 x 8-bit memory addressed by the four bits. Data stored in the color RAM selects a color for a pixel.

The content of the color RAM is set up initially, and changed during the game by the MPU. When the MPU writes to the color RAM, function $\overline{E5}$ (Enable 5 Not) is produced to select MPU address bits A0 through A3 through the address multiplexer, and the state of MPU data bits DO through D3 are written into the desired color RAM location.

The 8-bit output from the color RAM is applied to the video D-to-A driver. Three bits define seven intensities for the Red gun, three bits for seven intensities of the Green gun, and the remaining two bits for three intensities of the Blue gun.

The Monitor Sync Generator decodes video outputs from the Video Address Bus to produce horizontal and vertical sync pulses for the Color Monitor. The Horizontal Blanking circuit also decodes Video Address Bus outputs to blank the Color Monitor at the left and right edges of the screen. The Video RAM corresponding to these areas are available to the MPU for "scratchpad" RAM, and the horizontal blanking overlaps the internal Color Monitor horizontal retrace blanking to prevent display on the Color Monitor.

The program is able to determine the vertical position of the scan on the screen at any time by reading the Vertical Count Buffer. Function $\overline{E7}.\overline{PS0}$ (Enable 7 Not AND Page Select 0 Not) latch the higher order Video Address Bus bits onto the MPU data bus for reading.

In addition, when the trace reaches the bottom of the screen, count 240 is decoded from the Video Address Bus and applied to an I/O (Input/Output) port on the ROM Board to produce an MPU Interrupt. Also, Video Address Bit All is applied to the I/O port on the ROM Board to produce a 4 mSec Interrupt.

The Page 0 decoder is provided with Page 0 select functions from the ROM Board and MPU Address leads and enables MPU access to the Interface Board 110, the Vertical Count Buffer, CMOS RAM, and the color RAM. The MPU reads and writes to the Interface Board and CMOS RAM, reads the Vertical Count Buffer, and writes to the color RAM.

The CMOS RAM is provided with standby battery power to maintain audit information and game adjustments. The CMOS RAM provides 256 4-bit memory locations. Audit information stored in the lower half of the memory, is written to as a part of game operation, and is read from as part of the high score signature attract mode. Game adjustments are stored in the upper half, and during game operation are only read. A "memory protect" switch is held closed when the coin door is closed to provide the Memory Protect function. This prevents writing to the upper half of the memory when the coin door is closed. With the coin door open, writing to the upper half is allowed so that changes to adjustments can be made.

Pages are selected by writing to $D000_{16}$ with data to select one of up to 10 pages. Address decoding provides chip-selects for the ROMs, for the inputs, and PIA. The ROM Board PIA scans coin door switches and provides outputs to the Sound Board. This PIA also provides outputs for the diagnostic LEDs. The 4 mSec and Count 240 functions from the CPU/Video Board produce interrupts to the MPU. The Model Interface Board accepts inputs from player panel switches through a PIA. The Page 0 Decoder on the CPU/Video Board provides a select-input for the PIA.

SECTION 3 DETAILED THEORY

RESET CIRCUIT (Figure 3-1)

The Reset Circuit ensures orderly start-up and recovery of the game by forcing a reset in response to any of the following situations:

1. Power-up (Unit is turned on or power failure has ended).
2. Power-down (Unit is turned off or power failure has occurred).
3. Reset pushbutton on CPU/Video board is depressed.
4. Low line or power supply voltage.

A Reset causes the MPU to start at the proper memory location, disables the CMOS RAM until the MPU is stable, forces all PIA ports to inputs, and synchronizes both the Video Address Generator and the 6MHz clock with the E clock.

Two signals are used for the Reset function: $\overline{\text{RESET}}$ (Reset Not), and $\overline{\text{CR}}$ (Clocked Reset Not). The $\overline{\text{RESET}}$ pulse width (approximately 1 second) is determined by the RC time constant R2/C1. $\overline{\text{CR}}$ is clocked high after $\overline{\text{RESET}}$ goes high by the next rising edge of the E clock, ensuring that the Video Address Generator and 6MHz divider are synchronized with the E clock when $\overline{\text{CR}}$ goes high.

When power is applied, C1 begins to charge through R2. At this point transistors Q4, Q5, Q1, & Q2 are all off. This allows R10 to pull $\overline{\text{RESET}}$ low, asserting the reset function. Since the $\overline{\text{CL}}$ (Clear Not) input of the data latch which generates $\overline{\text{CR}}$ is tied to $\overline{\text{RESET}}$, its Q output is forced low, asserting $\overline{\text{CR}}$.

As the charge on C1 reaches approximately 0.9 VDC, Q1 is biased on through R1 and R3. This has no immediate effect, but enables Q2, which will be turned on later. C1 continues to charge, and at approximately 3.0 VDC biases on Q4. As Q4 begins to conduct, it pulls its collector current through R4 and R6, increasing the voltage drop across these resistors. When the voltage drop across R6 increases to 0.7 VDC, Q5 is biased on and starts to pull $\overline{\text{RESET}}$ toward +5 VDC.

Since Q1 was turned on earlier, there is a current path to ground from the emitter of Q2, causing Q2 to turn on as the voltage on $\overline{\text{RESET}}$ rises. Once Q2 turns on, its collector draws current through R17, increasing the base current of Q5. At this point Q2 and Q5 continue to increase each other's base drive until both transistors are saturated, latching each other in this condition.

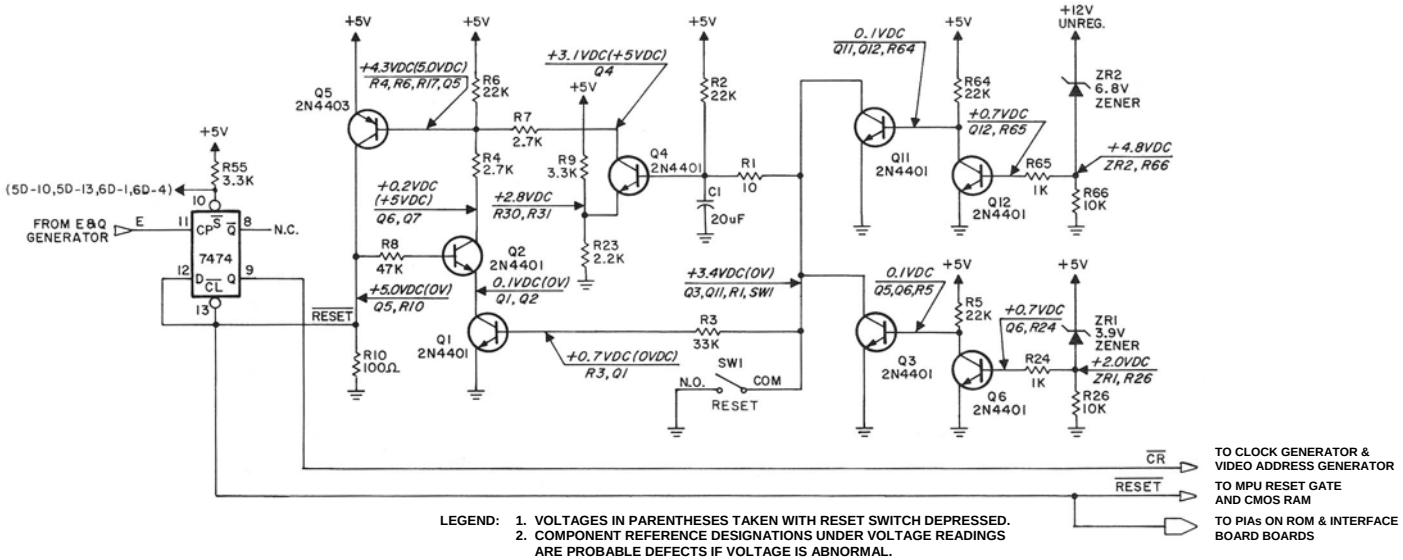

Figure 3-1. Reset Circuit

The purpose of this latch is ,to provide a fast transition of $\overline{\text{RESET}}$ from its asserted (low) state to its negated (high) state.

With $\overline{\text{RESET}}$ high, $\overline{\text{CR}}$ will go high at the next rising edge of E clock, which clocks the high present at the D input of the data latch out to the Q output.

Depressing Reset switch, SW1, shorts the charge on C1 to ground. This turns off both Q1 and Q4. When Q1 turns off it breaks the emitter circuit of Q2, forcing it off and breaking the Q2/Q5 latch effect. Since neither Q2 or Q4 is supplying base drive to Q5, it turns off, allowing $\overline{\text{RESET}}$ to be pulled low by R10, forcing CR low. When the Reset button is released, C1 begins to charge again. From this point, the circuit operates as described in the power-up sequence.

The power-down sequence is triggered by either the +12 VDC unregulated supply or the +5 VDC regulated supply dropping below acceptable limits. Since the operation of the sensing circuits is similar, only the +12 VDC sensor is described.

During normal circuit operation, ZR2 is biased on, but is operated close to its turn-off point by R66. Some of the current flowing through ZR2 also flows through R65, biasing Q12 on. The collector of Q12 pulls the base of Q11 down to 0.1 VDC, forcing Q11 off.

When a power-down (or voltage drop) occurs, ZR2 stops conducting as the supply voltage drops. This removes the base bias of Q12, turning it off and allowing R64 to bias Q11 back on. This has the same effect as pushing the reset button, shorting the charge on C1 to ground, thereby asserting reset outputs $\overline{\text{RESET}}$ and $\overline{\text{CR}}$.

WATCHDOG CIRCUIT (Figure 3-2)

The Watchdog Circuit is a timer which resets the MPU if it is not cleared at least once every 133 mSec. To clear the watchdog timer, the MPU writes a specific data byte (38_{16} or 39_{16}) into address $C3FF_{16}$ with page 0 selected. The game program is designed to perform this clear operation regularly, ensuring that the watchdog will not reset the MPU during normal operation.

Noise transients and other problems will sometimes cause an MPU to jump out of the normal program sequence. If this happens the MPU will often misinterpret

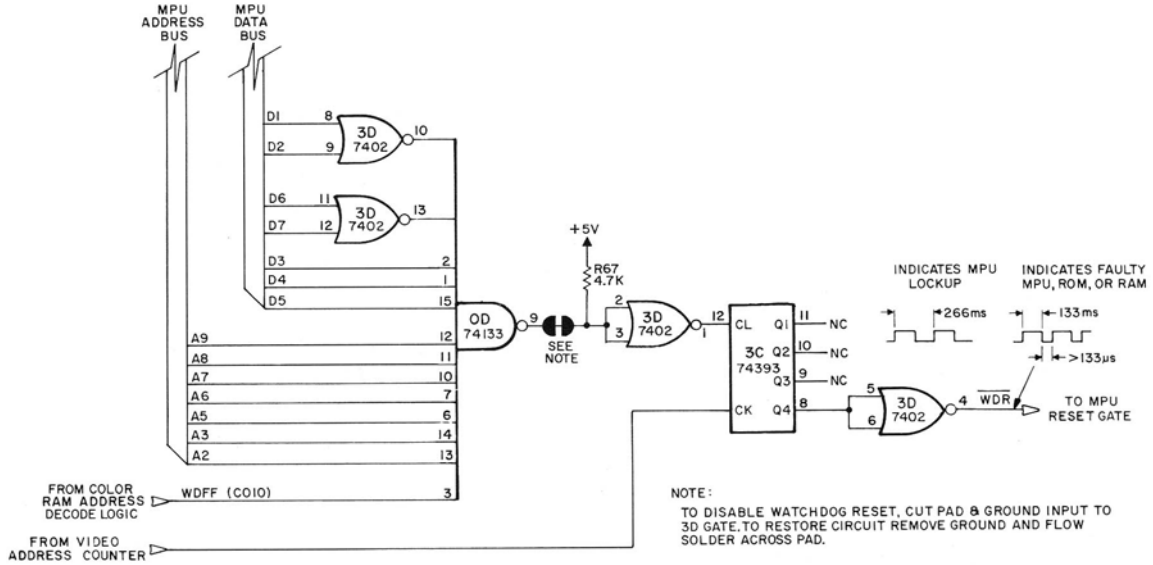

Figure 3-2. Watchdog Circuit